Circuit Suitable for Use in a Carry Lookahead Adder

ABSTRACT

An adder circuit for determining the sum of two operands including a set of PGK circuits, at least one tier of group circuits, and a carry generation circuit. The PGK circuits are configured to generate propagate, generate, and kill bits corresponding to at least a portion of the first and second operands. The group circuit receives propagate, generate, and kill bits from a plurality of the PGK circuits and produces a set of group propagate, generate, and kill values. The carry generation circuit receives a carry-in bit and the outputs of at least one of the group circuits and generates a carry-out bit representing the carry-out of the corresponding group. Each generate bit is the logical AND of its corresponding bits in the first and second operand while each propagate bit is the EXOR of its corresponding bits, and each kill bit is the logical NOR of its corresponding bits. At least one of the PGK circuits, group circuits, and carry circuits may be implemented with CMOS transmission gates in lieu of conventional complementary pass-gate logic (CPL). The PGK circuits and groups may further generate true and complement output signals substantially simultaneously.